Faculty of Engineering

PERFORMANCE OF SCHMITT TRIGGER

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PERFORMANCES OF SCHMITT TRIGGER

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(Supervisor)

Dedicated to my beloved parent and family, lecturers and friends.

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ABSTRAK

Dalam projek ini, ciri-ciri rekaan dan nisbah lebar terhadap panjang bagi transistor mempengaruhi keupayaan bagi litar “Schmitt Trigger”. Usul rekaan ini direka berdasarkan litar “Schmitt Trigger” yang sedia ada iaitu “Conventional CMOS Schmitt Tigger” dengan memanipulasikan susunan transitor serta nisbah lebar terhadap panjang. Seterusnya, analisa dijalankan terhadap ketiga-tiga litar rekaan dengan menggunakan “Microwind” berdasarkan kepelbagaian nilai kapacitor dan sumber voltan. Akhir sekali, perbandingan antara ketiga-tiga litar rekaan akan dianalisa dari segi “propagation delay”, “Power-Delay Product” dan “hysteresis voltage”.

ABSTRACT

In this project, the designs and the width-length ratio of the transistors affects the performances of the Schmitt Trigger circuit. The proposed design is designed based to the existing Schmitt Trigger which is the Conventional CMOS Schmitt Trigger by manipulating the arrangement of transistors and the width-length ratio. Then, analyses are conducted on the three designs using Microwind at variations of load capacitance and source voltages. Lastly, comparisons are made between the three designs in term of propagation delay, Power-Delay Product and hysteresis voltage.

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ABBREAVIATIONS

BJT	Bipolar Junction Transistor
CMOS	Complementary Metal-Oxide Semiconductor Field-Effect Transistor
DRC	Design Rule Checker
GND	Ground
IC	Integrated Circuit
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	N-channel MOSFET
PDN	Pull-down Network
PDP	Power-Delay Product
PMOS	P-channel MOSFET
PTL	Pass Transistor Logic
PUN	Pull-up Network
VTC	Voltage Transfer Characteristic

CHAPTER 1

INTRODUCTION

1.1 Introduction

Schmitt Trigger circuit is normally introduced to a logic gate or circuit to overcome noisy input signal into the logic gate (or circuit). A noisy input signal causes unwanted changes, which may influence the performances of the logic gate (or circuit). Hence, Schmitt Trigger overcomes this problem by introducing two switching threshold voltages.

As a noisy signal is inputted to the trigger circuit, its output state will changed when its input voltage level rises above a switching threshold voltage. Then, the output state will be switched back automatically once the input voltage level sinks below a lower switching threshold voltage. As a result, the output state only comprises two levels, high and low. Thus, noisy input signal can be minimized.

1.2 Objectives

The main objectives of the project are as follows:

1.2.1 To design a Schmitt Trigger Circuit

The Schmitt Trigger circuit will be designed based on the conventional CMOS Schmitt Trigger by manipulating the pull-up network design as it gives a greater effect to the performances of the Schmitt Trigger compare to the pull-down network.

1.2.2 To analyze the performance of the proposed Schmitt Trigger Circuit

The performances of the circuit are being analyzed in term of delay and power consumption using Microwind. This project also studies the characteristic of the circuit when the input is high and low. In addition, the Voltage Transfer Characteristic will be plotted and analyzed.

1.2.3 To analyze and compare Schmitt Trigger Circuits

Once the Conventional CMOS Schmitt Trigger's characteristic is understand, the circuit will be analyzed in term of its performances and hysteresis width. Then both the Schmitt Trigger circuits' (conventional CMOS and proposed Schmitt Trigger) performances and hysteresis width are compared.

1.3 Outlines of Project Report

This project report is divided into five chapters. The first chapter is mainly on introduction of the project and the objectives.

Chapter 2 focuses on the studies of Voltage Transfer Characteristic of the Schmitt Triggers according to the types and the characteristics of conventional CMOS Schmitt Trigger circuit. It will also cover the method used in designing and analysis of the performances of the Schmitt Trigger Circuits.

The methodology in designing will be discussed in Chapter 3. In addition, this chapter will explained the program used in simulating the design, which is the Microwind software. The studies of the characteristic of the designed circuit will be discussed in this chapter as well.

The simulation result will be discussed in Chapter 4. Furthermore, comparison between the performances of the proposed circuit with Conventional Schmitt Trigger will be discussed in this chapter.

Chapter 5 concludes the design and performances of the proposed Schmitt Trigger circuit. It also contains recommendation for future improvement.

CHAPTER 2

LITERATURE REVIEW

2.1 The History of Schmitt Trigger

The Schmitt Trigger circuit (which previously was known as "Thermionic Trigger") was founded by Otto Herbert Schmitt, an US scientist [5]. The circuit is shown in Figure 2.1 and is known as Emitter Coupled Binary Trigger Circuit.

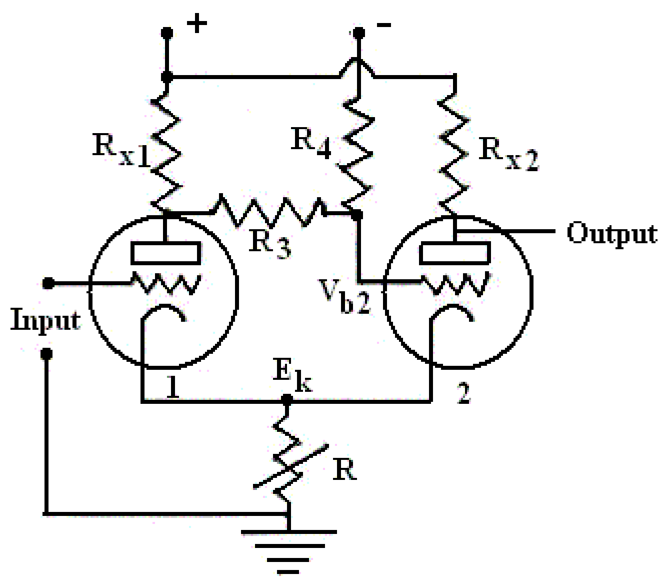

Figure 2.1 The Thermionic Trigger Circuit

The circuit is termed as binary trigger circuit because only one BJT will be on at one time. When input is low, Q1 has no forward bias and is cutoff. Since the collector voltage for Q1 is high, thus Q2 is on. Based on equation 2.1, V_{b2} is slightly positive potential relative to the emitter thus Q2 operates in saturation region. The emitter current of Q1 flows through R and produces V voltage across R. Since the base of Q1 is low, the base or emitter junction of Q1 is reversed biased by V volt. Q1 will be on when the input signal exceed its threshold voltage. A low input causes a high output and vice versa when the input is high.

$$V_{b2} = \frac{R_4}{R_{x1} + R_3 + R_4} V_{DD} \qquad (2.1)$$

The difference between the values of Q1 base voltage turned on and off is known as hysteresis.

2.2 Schmitt Trigger

Schmitt trigger is a device with two important properties [6]. Firstly, it responds to a slowly changing input waveform with a fast transition time at the output and secondly, the voltage-transfer characteristic (VTC) of the device shows the switching thresholds for both positive- and negative- going input signals.

The characteristic curve for both inverted and non-inverted Schmitt Trigger will be discussed in section 2.2.1 and 2.2.2. The upper and lower switching thresholds are labeled as V_{TH} and V_{TL} and are obtained from the intersections of the VTC curve with the $V_{output} = V_{input}$ line. The difference between the two switching threshold voltages is known as hysteresis voltage and can be obtained from the equation 2.2. Hysteresis helps in reducing noise effect in a system as it is less sensitive to minute of changes in the input voltage in the vicinity of two switching threshold voltages. According to [1], a small difference in both the switching threshold voltages will be less tolerant to noise while if the difference is large, it has a more muted response. Thus, the Schmitt Trigger circuit should be designed ideally to give the best performances.

$$\Delta V_T = V_{TH} - V_{TL} \tag{2.2}$$

Generally, a circuit desires a switching threshold located around the middle of the available voltage swing (or at $\frac{1}{2}V_{DD}$) because this causes the values for low and high noise margins to be comparable. However, asymmetrical transfer characteristics are desirable in a Schmitt Trigger and can be obtained by manipulating the PMOS and NMOS width ratio. The effect of changing the ratio is to shift the transient region of the VTC[6] where an increased of the PMOS's or NMOS's width will moves the switching threshold towards V_{DD} or ground. Therefore, this can increase the hysteresis width of the Schmitt Trigger which is more sensitive to noise.

2.2.1 The Voltage Transfer Characteristic for an Inverting Schmitt Trigger

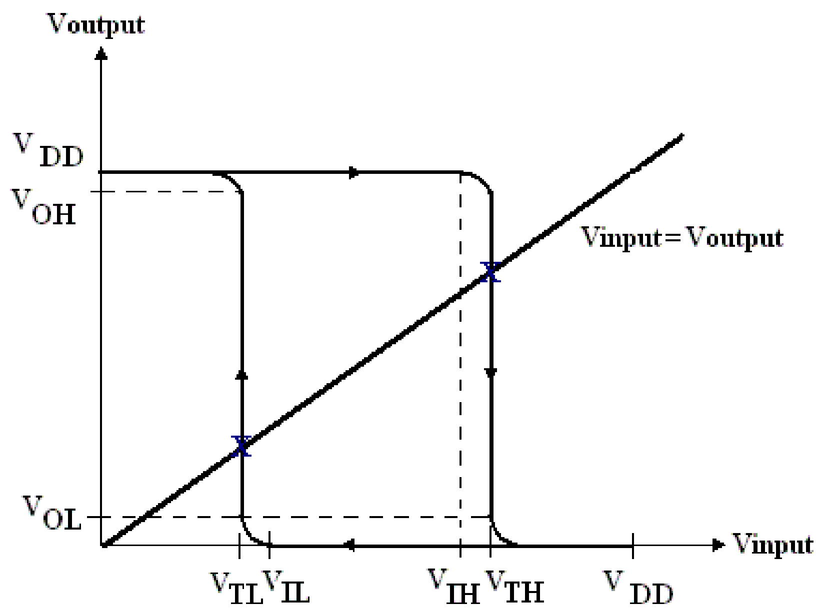

Figure 2.2: The Transfer Characteristics of an Inverting Schmitt Trigger

From Figure 2.2 and according to [3], when the input is low at V_{IL}, the circuit saturates to V_{OH}. As the input increases, it moves the operating point along the upper